**PATENT** 



## ATTORNEY DOCKET NO.: Intel 2207/10121 ASSIGNEE: INTEL CORPORATION

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICANTS** 

Sailesh KOTTAPALLI et al.

RECEIVED

SERIAL NO.

09/751,762

SEP 2 2 2004

**FILED** 

December 29, 2000

**Technology Center 2100** 

**FOR** 

METHOD FOR CONVERTING PIPELINE STALLS

CAUSED BY INSTRUCTIONS WITH LONG LATENCY MEMORY ACCESSES TO PIPELINE FLUSHES IN A MULTITHREADED PROCESSOR WHERE THE

INSTRUCTIONS ARE RE-EXECUTED UPON

**COMPLETION OF THE ACCESSES** 

GROUP ART UNIT:

2183

**EXAMINER** 

Shane F. GERSTL

M/S: AMENDMENTS Commissioner for Patents PO Box 1450

Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: M/S: AMENDMENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: September 14, 2004

Signature\_

Pilar Rodriguez

## **RESPONSE**

The following amendments and remarks below are respectfully submitted in response to the Office Action dated June 3, 2004.

Listing of the Claims begin on page 2 of this response.

Remarks/ Arguments begin on page 6 of this response.

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